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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
VOCKRODT, JEFF B	

ART UNIT	PAPER NUMBER
2822	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/160,657	LYDING ET AL.	
	Examiner	Art Unit	
	Jeff Vockrodt	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 June 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *40,41,47,60-65 and 76-84* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *40,41,47,60-65 and 76-84* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☒ Interview Summary (PTO-413) Paper No(s). *46* .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

This office action is in response to the amendment filed May 13, 2003 and the supplemental response filed June 4, 2003. Claims 66-74 were cancelled in the amendment filed July 8, 2003. The attached interview summary indicates that claims 66-74 would be cancelled to avoid a notice of non-responsive amendment. Applicants July 8, 2003 amendment effects that cancellation. Claims 40-41, 47, 60-65, and 76-84 are pending.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 81-82 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lisenker in view of U.S. Pat. No. 5,434,440 ("Yoshitomi").

> 81. (New) An improved semiconductor device including an insulated gate field effect transistor device having a transistor gate and a gate insulator film not exceeding about 55 Angstroms thickness interposed between said transistor and a channel of said transistor device and a concentration of deuterium introduced into and remaining within said film, said transistor device susceptible to degradation associated with hot carrier stress, said concentration of deuterium substantially reducing said degradation associated with said hot carrier stress.

Claim 81 reads on a transistor having a gate oxide thickness of less than or equal to about 55 angstroms (5.5nm) in which deuterium has been provided in an amount sufficient to reduce degradation associated with hot carrier stress. Claim 81 does not require post-metal annealing, but merely requires a concentration of deuterium remaining in the film.

Lisenker teaches annealing a MOS gate oxide film with deuterium to add deuterium to the silicon oxide film. Lisenker teaches adding deuterium in a quantity sufficient to increase the ratio of deuterated to hydrogenated bonds to greater than about 99:1 (page 11). Lisenker teaches that where hydrogen is used to remove dangling bonds at the Si/SiO_2 interface in

transistor gate oxides, page 2, ll. 10-25, substitution of hydrogen with deuterium results in transistors having improved stability, quality, and reliability, page 4, ll. 32-34. Lisenker differs from claim 81 by not teaching the thickness of the gate oxide layer and therefore differs from the claimed range of less than 55 angstroms.

Yoshitomi establishes that CMOS FETs having a gate oxide thickness not exceeding 55 angstroms (5.5nm) were well known at the time of applicant's invention. Specifically, Yoshitomi teaches growing a gate oxide (27l Fig. 29C) having a thickness of 4nm (40 angstroms) (Yoshitomi; col. 16, ll. 30-35). One of ordinary skill in the art would recognize that thinner gate oxides are desirable since they lower the operating voltage of the device. It would have been obvious to one of ordinary skill in the art at the time of the invention to produce a gate oxide thickness of 4nm in the device of Lisenker to scale down the operating voltage.

Claim 82. The gate insulator is silicon oxide as discussed above.

Claims 40-41, 60, and 61 are rejected under 35 U.S.C. 103(a) as being unpatentable over any one of Deal, Paivinen, Taguchi, or Cederbaum in view of WO 94/19829 ("Lisenker").

Post metal annealing using a hydrogen and nitrogen mixture, otherwise known in the art as forming gas, is a standard procedure that is applied to NMOS devices in the prior art. The following references are listed chronologically as of their filing date (the significance of the chronology will be discussed in conjunction with claims that include a gate oxide thickness limitation).

1) U.S. Pat. No. 4,027,380 ("Deal"). Deal teaches a post-metallization anneal using hydrogen at 300-500°C on a CMOS (both NMOS and PMOS) device (col. 9, ll. 33-53). Deal explains that the purpose of the post metal anneal is to minimize the fast interface state density which adversely affects threshold voltages. Deal does not appear to teach a gate oxide thickness. Filed January 16, 1977.

2) U.S. Pat. No. 4,212,100 ("Paivinen"), col. 7, ll. 5-10. Paivinen teaches post aluminum sintering in forming gas (10% H, 90%N, 5 minutes, 400°C) to provide improved metallurgical bonding between the aluminum and the polysilicon portions remaining on the substrate. Paivinen teaches an NMOS device. The gate oxide thickness is 1000 angstroms (col. 6, ll. 9-14). Filed September 23, 1977.

4) U.S. Pat. No. 5,198,880 ("Taguchi"), col. 4, ll. 39-45. Taguchi teaches post aluminum metallization annealing in forming gas at 450 °C after forming CMOS devices (both PMOS and NMOS). The gate oxide thickness is 700 angstroms (col. 3, last paragraph). Continuation of application filed June 19, 1990.

5) U.S. Pat. No. 5,320,975 ("Cederbaum"). Cederbaum teaches post annealing (at any subsequent level) in a forming gas (hydrogen and nitrogen mixture, 400°C for 30 minutes) applied to a CMOS (both PMOS and NMOS) array. Cederbaum explains that hydrogen passivation of dangling bonds is effected by the forming gas anneal. (Cederbaum, paragraph bridging cols. 13-14.) The gate oxide thickness is 10nm (100 angstroms) (col. 10, ll. 8-10). Filed March 22, 1994.

Lisenker teaches "improved VLSI fabrication methods that minimize some of the detrimental effects associated with hydrogen in oxides." (Lisenker, page 1). One of the effects that Lisenker is concerned with is "high sensitivity to hot carrier degradation," which Lisenker states can result from increased surface states at the silicon surfaces caused by uncompleted or "dangling" silicon bonds, increased fixed charge on the silicon/silicon dioxide interface, and vacancies in the bulk oxide. (Lisenker, page 1.) Lisenker discusses the beneficial effects of hydrogen tying up some dangling bonds at the silicon/silica interface, but due to the weak Si-H bonds, the number of dangling bonds increases with the free hydrogen migrating away. (Lisenker, pages 2-3.) (this phenomenon is explained by applicants as hydrogen depassivation) Lisenker discusses the problem of "hot" electrons, which are a source of stress that leads to increased dangling bonds. (Lisenker, page 4.) Generally, Lisenker teaches solving these problems by replacing "any hydrogen containing material used in VLSI fabrication" with a "corresponding deuterium containing material." (Lisenker, page 4, ll. 32-34.) Although it is not a post metal anneal, Lisenker does teach annealing in deuterium at a temperature of about 500°C for approximately 10 to 20 minutes (Lisenker, page 9, ll. 15-25).

Lisenker is relevant to applicant's invention because Lisenker is concerned with the problem of hot carrier degradation, which is the problem that applicant's invention addresses. Deal, Paivinen, Taguchi, and Cederbaum are relevant because they employ hydrogen

annealing to transistor devices and would suffer from some of the problems discussed by Lisenker.

The claimed invention:

> 40. A semiconductor device comprising an n-channel field effect transistor including a drain formed in a semiconductive layer, a source formed in said semiconductive layer, a channel extending between the drain and the source, a gate insulating layer over said channel, an interface between a semiconductive silicon layer and a gate insulating layer, and conductive contacts to said drain, source and on said gate insulating layer, said field effect transistor structurally characterized by the retention of deuterium at said interface resulting from post-fabrication passivation of said interface in a heated, deuterium gas-enriched atmosphere at a temperature of about 200°C to about 1000°C so as to increase the resilience of the field effect transistor to hot electron effects during operation.

The only difference between claim 40 and any one of Deal, Paivinen, Taguchi, or Cederbaum is that these references employ hydrogen annealing instead of deuterium annealing. Lisenker teaches that switching from hydrogen to deuterium will add deuterium into the device, which is useful for solving problems that result from using hydrogen. One of those problems is high sensitivity to "hot" carrier effect--the same problem that applicant solves.

Neither criticality nor unexpected results are shown for post annealing in deuterium (claimed invention) relative to annealing in deuterium before contacts are formed. The data in the specification, including Figs. 2-3, compares annealing in deuterium relative to annealing in hydrogen. Annealing in hydrogen is not the closest prior art. The closest prior art reference is Lisenker. Applicants have not shown that annealing post-metallization in deuterium is critical or has unexpected results relative to pre-metal annealing in deuterium (i.e., Lisenker).

Lisenker's teaching would motivate one of ordinary skill in the art to replace the hydrogen in the post metal hydrogen anneal in any one of Deal, Paivinen, Taguchi, or Cederbaum with deuterium. Based on Lisenker, one would expect this modification to result in beneficial deuterium being incorporated into the device rather than hydrogen.

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the conventional post-metal hydrogen anneal (i.e., any one of Deal, Paivinen,

Taguchi, or Cederbaum) to replace the hydrogen with deuterium as suggested by Lisenker. One of ordinary skill in the art would have expected that this modification would provide some improvement in sensitivity to hot carrier degradation as taught by Lisenker.

Claims 41 and 60-61. The gate oxide in all of the references is silicon dioxide.

Claims 62-63, 65, 76-82, and 84 are rejected under 35 U.S.C. 103(a) as being unpatentable over any one of Deal, Paivinen, Taguchi, or Cederbaum in view of Lisenker as applied to claims 40-41, 60 and 61 above, further in view of Yoshitomi.

Claims 62-63, 65, 76-82, and 84 differ from the combination of any one of Deal, Paivinen, Taguchi, or Cederbaum in view of Lisenker by requiring a gate oxide thickness of less than 55 angstroms (5.5 nanometers). Deal does not teach a gate oxide thickness and Paivinen, Taguchi, and Cederbaum each teach gate oxide thickness of 1000, 700, and 100 angstroms respectively. The issue presented by the present claims is whether it would have been obvious to one of ordinary skill in the art at the time of applicant's invention (the day before January 16, 1996) to modify the post metallization deuterium anneal that is suggested in the prior art by applying it to a transistor having a gate oxide thickness of less than 55 angstroms. That gate oxide thickness is being made thinner over time is shown by Paivinen, Taguchi, and Cederbaum. Since there is ample motivation to decrease gate oxide thickness, the question is then whether gate oxide thickness of less than 55 angstroms were available at the time of the invention.

Yoshitomi establishes that CMOS FETs (including NMOS) having a gate oxide thickness not exceeding 55 angstroms (5.5nm) were known at the time of the invention. Specifically, Yoshitomi teaches growing a gate oxide (27, Fig. 29C) having a thickness of 4nm (40 angstroms) (Yoshitomi; col. 16, ll. 30-35). The trend of decreasing gate insulator thickness in CMOS devices and transistors in general correlating to decreased operation voltage is well known and provides a motivation to use thinner gate oxide thickness when fabricating a transistor devices. Applicant has not shown that the gate oxide thickness is critical to achieve

unexpected results. The prior art that the invention is compared to in the specification is not the closest prior art (i.e., it is not equivalent or cumulative to Lisenker) and there is no logical basis for finding criticality with respect to Lisenker the closest prior art for the gate oxide thickness limitation.

It would have been obvious to one of ordinary skill in the art at the time of the invention to provide the device taught by Deal, Paivinen, Taguchi, or Cederbaum in view of Lisenker with a gate oxide thickness of less than 55 angstroms (specifically 40 angstroms as taught by Yoshitomi). One of ordinary skill in the art would have been motivated this known gate oxide thickness by the general trend of decreasing gate oxide thickness such that a lower operating voltage may be obtained.

Claim 65. The deuterium atoms are covalently bonded according to Fig. 1 of Lisenker.

Claim 79. Claim 79 requires "said post-fabrication passivation being conducted sufficiently to provide to said transistor a practical lifetime at least about ten times that provided by a corresponding passivation with hydrogen, wherein practical lifetime is takes as 20% transconductance degradation as a result of electrical stress." This is simply a result of the process of forming the device, which has been found to be obvious as discussed above.

Claims 80-82 and 84. The limitations of these claims have been discussed above and are obvious for the same reasons.

Claim 47 is rejected under 35 U.S.C. 103(a) as being unpatentable over Deal, Paivinen, Taguchi, or Cederbaum in view of Lisenker as applied to claims 40-41, 60 and 61 above, further in view of U.S. Pat. No. 4,435,896 ("Parrillo").

Claim 47 differs from Deal, Paivinen, Taguchi, or Cederbaum in view of Lisenker as applied to claims 40-41, 60 and 61 above by requiring encapsulation.

Parrillo shows that a silicon nitride passivation layer (90) is deposited over the metallization (89) after the post metallization anneal in hydrogen (col. 6, ll. 6-19).

It would have been obvious to one of ordinary skill in the art at the time of the invention to deposit a silicon nitride layer over the metallization of Deal, Paivinen, Taguchi, or Cederbaum in view of Lisenker to passivate the device as taught by Parrillo.

Claims 76-78 are rejected under 35 U.S.C. 103(a) as being unpatentable over Deal, Paivinen, Taguchi, or Cederbaum, Lisenker, and Yoshitomi as applied to claims 40-41, 60-63, 65, 76-82, 84 above , further in view of U.S. Pat. No. 4,796,081 ("Cheung").

Claim 76 requires an anneal of 10% deuterium, 90% nitrogen, at 400°C, for one hour. Claim 76 differs from the applied prior art by requiring a duration of one hour.

Cheung teaches that post metal sintering in forming gas is typically conducted at 400-450°C and a duration of between 45minutes to 2 hours. The claimed ranges are within or overlapping the prior art conditions for post-metal forming gas anneals. There is nothing in the specification suggesting unexpected results for the claimed duration ranges. It would have been obvious to one of ordinary skill in the art at the time of the invention to select an anneal duration of one hour at 450°C using a 10% hydrogen 90% nitrogen composition as claimed since these values were well known forming gas parameters as shown by Cheung.

Claims 77-78. The gate insulator is silicon oxide, the semiconductor material is silicon.

Claims 64 and 83 are rejected under 35 U.S.C. 103(a) as being unpatentable over Deal, Paivinen, Taguchi, or Cederbaum, Lisenker, and Yoshitomi as applied to claims 40-41, 60-63, 65, 76-82, 84 above, further in view of U.S. Pat. No. 5,254,506 ("Hori").

Claims 64 and 83 requires a silicon oxynitride gate insulator.

Hori teaches a silicon oxynitride gate insulator being used in place of a silicon oxide gate insulator having the advantage of greater dielectric strength (higher dielectric constant) without sacrificing mobility.

It would have been obvious to one of ordinary skill in the art at the time of the invention to use silicon oxynitride as a gate insulator in the device taught by Deal, Paivinen, Taguchi, or

Cederbaum in view of Lisenker to increase the dielectric constant while maintaining sufficient mobility as taught by Hori.

Response to Arguments

Applicant's arguments filed May 13, 2003 and June 4, 2003 have been fully considered. To the extend that these arguments have applicability to the new grounds of rejection presented in this office action, they are not persuasive.

Enomoto teaches post fabrication annealing in a DRAM. The examiner has withdrawn Enomoto. Applicant asserted that DRAMs did not come within the claimed gate oxide thickness at the time of the invention. The examiner agrees and has withdrawn Enomoto (for the claims that are not limited to gate oxide thickness Enomoto is considered cumulative to the newly cited references and has been withdrawn on that basis). However, searching has revealed that post-metal annealing is not something that only pertains to DRAM fabrication. These references are relied on above to show post-metallization hydrogen annealing was relevant in CMOS processing as well. The new grounds of rejection are set out above.

Lisenker teaches annealing in deuterium before, during, and after forming a gate oxide. Lisenker does not specifically teach annealing post-metallization--indeed, if it did at least some of the claims would be anticipated. Applicant asserts that Lisenker should be understood as limited to annealing to introduce deuterium only in pre-metallization anneals. Lisenker does not say this. Lisenker does include a specific embodiment that is not a post-metallization anneal. However, Lisenker is available for all that it would suggest to one of ordinary skill in the art. Applicants only textual basis for limiting Lisenker comes from Lisenker's specific embodiment. There is no teaching away from post-metal deuterium annealing in Lisenker. In fact, Lisenker clearly envisions anneals at other times during the fabrication process. In this connection, Lisenker states "The present invention can be implemented throughout the VLSI fabrication procedure." One of ordinary skill in the art, aware of the litany of post-metal hydrogen annealing teachings for CMOS (e.g., Deal, Paivinen, Taguchi, or Cederbaum), would not limit the

importance of Lisenker in the manner suggested by applicant. This understanding of Lisenker is supported by substantial evidence.

The examiner would like to point out that there is insufficient evidence to conclude that applicant's results (i.e., the increased resistance to hot carrier degradation) has anything to do with post-metal annealing (the now claimed invention). The specification does not compare post-metal deuterium annealing (claimed invention) with pre-metal deuterium annealing (Lisenker). Instead, the only comparison made by applicant is with hydrogen annealing, which is not the closest prior art. Additionally, applicants state in their specification that benefits can be achieved by introducing deuterium at stages other than post fabrication. There came a time when applicant suggested on this record (response to office action #2, filed 08-02-99, page 4) that these results should be considered in the obviousness inquiry as part of the invention as a whole. In that same response, applicant suggested that Ipatova et al. acknowledged these large improvements. Ipatova, which is a reference of record, did not suggest that these improvements had anything to do with post-metallization annealing. In fact, Ipatova did not even acknowledge the existence of the closest prior art (Lisenker) when making these statements. Those who have recognized post-metallization annealing with deuterium, U.S. Pat. No. 6,328,801 ("Gary"), attribute the invention to Lisenker. (See paragraph bridging cols. 1-2.) Therefore, it is inconclusive whether (1) there are unexpected benefits for post-metal annealing in deuterium relative to the closest prior art and (2) whether others actually attribute those results to post-annealing rather than annealing at any other stage in the process. Accordingly, the disclosed results (i.e., Figs. 2-3) have been given little weight in the obviousness analysis.

Conclusion

The references made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Pat. No. 4,992,840 ("Haddad"). Haddad discusses hot carrier aging and attempts to solve the problem by including carbon at the silicon/silica interface. Notably, Haddad establishes that hot carrier effects were a problem for near-micrometer devices.

U.S. Pat. No. 5,822,175 ("Azuma"). Azuma teaches: "Post-metallization annealing in forming gas (N_2 - H_2, 1-25% H_2) in the temperature range of 350°-500°C is standard for aluminum line sintering." (col. 2, ll. 29-31).

Any inquiry concerning communications from the examiner should be directed to Jeff Vockrodt at (703) 306-9144 who can be reached on weekdays from 9:30 am to 5:00 pm EST. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian, can be reached at (703) 308-4905.

The fax numbers for this Group are (703) 305-3432, (703) 308-7722, (703) 305-3431, and (703) 308-7724. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist at (703) 308-0956.

September 11, 2003

J. Vockrodt

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